Second Design Review

SURFACE VEHICLE NAVIGATION STUDY (SVNS)

September 1979 to March 1980

Sponsored by
Frank Weinchel, Vice President
General Motors Technical Center
Warren, Michigan

Performed by
Rockwell-Collins
Avionics Advanced Technology
Avionics and Missiles Group
Cedar Rapids, Iowa

Steve F. Russell, Project Manager

In January of 1979, I transferred from the NAVSTAR GPS (GDM) program to the Advanced Technology Department of the Avionics and Missiles Group. It was a promotion step toward becoming a Principal Engineer. I wanted the freedom to work on a variety of projects instead of just one or two. I still continued my support of the GDM program and was heavily involved in its success.

For a year or more I had been talking to Rockwell leadership about transferring our military technology to the realm of civil applications of GPS. Primarily, I had in mind that we would develop GPS for civil aviation and automobiles. There was understandable resistance to the idea because our business expertise was military, not civil. However, the head of our advanced technology department, Norbert Hemesath, believed in the idea and began looking for an outside sponsor for a design and trade-off study for civil applications of GPS. He found support for the idea from Frank Weinchel, VP at General Motors.

GM funded us at a level of $840K/yr (2010 dollars) and we launched the SVNS project with a team of 7 engineers with varied expertise to do the trade-off study. This report summarized the majority of our work and was created to inform GM as to the feasability of putting a system in Cadillacs. My colleagues soon nicknamed the project 'CADNAV'.

Although I was the Project Manager, my instincts as a design engineer still drove me to participate in the system and function design as much as I could. I am especially happy to have had the time to develop the system concept represented in the diagram in this report. It was a logical extension of my experience on the GDM program.

There were many memorable moments on this project but none were more memorable than the trip to Warren, Michigan to present the progress report to Frank Weinchel; and the technical meetings with Wes Rogers and Jim Laggan. The minute I

arrived at the GM Tech Center, I was ushered into a room and given instructions on how I was to conduct myself, what I was to say and details on Frank's personality. You don't often encounter these issues in day-to-day engineering! I swear the following is exactly what happened. My Instructions were as follows:

1. Frank has an ulcer so we will not be serving alcohol at the meeting.
2. Don't mention anything about project problems to Frank.
3. Jim Laggan (my technical counterpart) will not be in the meeting because GM has a rule about how many levels of management can be in a room at the same time and Frank ranks too high for Jim to be in the meeting.

It was a whole new world as compared to the very formal engineering environment at Rockwell.

I left Rockwell-Collins for King Radio in August of 1980 and did not get to see the project to its completion. However, it was put into the very capable hands of my colleague, Jurgen Bruckner who did a great job of completing it.

Steve F. Russell
Project Manager, SVNS

REFERENCE: Memo, SVNS-12, March 21, 1980

Here is a list of the names of people I remember from that project:

Loren DeGroot
Norbert Hemesath
Robert 'Bob' Pool
'Ab' Mayer
Dave Cunningham
Robert 'Bob' Jaycox
John 'Jack' Murphy
Lew Nigra
Jurgen Bruckner
Ken Brown
Eugene 'Gene' Frye
Robert 'Wade' Walstrom
Howard Rooks

2nD DesiGN Review
&
SVNS PROGRAM Review

SVNS DISTRIBUTION

Date: 21- MARCH- 1980

Memo: SVNS - 12

X GROUP-1

		L. E. DeGroot	107-142
		N. B. Hemesath	124-222
		R. H. Pool	124-222
		A. F. Mayer	106-180
		D. L. Cunningham	107-142
		R. L. Jaycox	107-141
(2)		S. F. Russell	124-222
		J. W. Murphy	107-142

GROUP-2

X	L. M. Nigra	106-180
	H. M. Schweighofer	124-222
	J. M. Bruckner	124-222
	M. H. Rhodes	106-187
	K. L. Brown	106-176
X	E. O. Frye	124-222
X	R. W. Walstrom	124-222
X	P. L. Roberts	107-142

GROUP-3

	H. B. Rooks	106-176
	J. A. Martin	106-176
	J. W. Donaldson	106-176

GROUP-4

	G. Griffith	107-142
	W. K. McCune	124-222
	N. K. Garnatz	120-123

3/19/80

Internal Letter

Rockwell International

Date: 21 March 1980

No:

TO: (Name, Organization, Internal Address)
Distribution

FROM: (Name, Organization, Internal Address, Phone)
S. F. Russell
124-222
X4911

Subject: SVNS Program Review

A program review for the SVNS study for GM was held in Warren, Michigan on Friday, March 14. A copy of the view cell handout is enclosed.

The purpose of the meeting was to inform the GM Tech Center VP, Frank Weinchel, of the status of the study. A secondary purpose was to discuss technical details with Wes Rogers and Jim Laggan. The schedule and manning view cells and the cost estimates on page 2,20 were not shown. Also, the Engineering Design Review (Section III) was not presented or discussed. Wes Rogers has informed me that he and Jim Laggan will present a written response to Section III.

The meeting was quite unproductive from a technical standpoint but did produce positive results about our effort and possible future work.

S. F. Russell Steve H. Russell
Project Manager

SFR/ljp
Attachment

056-0010-020
Form 131-R (Rev 3-79)

SURFACE VEHICLE NAVIGATION SYSTEM

PROGRAM REVIEW

14 MARCH 1980

ROCKWELL INTERNATIONAL
AVIONICS AND MISSILES GROUP

I, NAVSTAR PROGRAM STATUS

AGENDA

I. NAVSTAR PROGRAM STATUS

II. EXECUTIVE SUMMARY

III. ENGINEERING DESIGN REVIEW

II. EXECUTIVE SUMMARY

EXECUTIVE SUMMARY

AGENDA

A. INTRODUCTION

B. PROGRAM OVERVIEW

C. MINIMUM-COST DESIGN

D. MINIMUM-COST DESIGN APPROACH

1) SVNS SYSTEM CONCEPT
2) BASELINE DEFINITION
3) ENGINEERING REVIEW
4) MAJOR HARDWARE COST ELEMENTS
5) COST AND PERFORMANCE TRADE-OFF STUDIES
6) RISK AREAS

E. ALTERNATE FUNCTIONAL DESIGNS

F. COST PREDICTIONS

G. TECHNICAL SUMMARY

INTRODUCTION

PROGRAM OVERVIEW

- PRINCIPLE OBJECTIVE
- STUDY OUTPUT
- STUDY OVERVIEW

PRINCIPLE OBJECTIVE

DEFINE A GPS-BASED SVNS WHICH:

1) MEETS ALL OF GM'S OPERATIONAL AND PERFORMANCE REQUIREMENTS FOR VEHICULAR USE AND

2) HAS THE POTENTIAL TO ACHIEVE THE STRINGENT COST GOALS ATTENDANT TO THE AUTOMOTIVE MARKET.

A. OPERATIONAL REQUIREMENTS
B. PERFORMANCE REQUIREMENTS
C. COST GOALS
D. AUTOMOTIVE APPLICATION

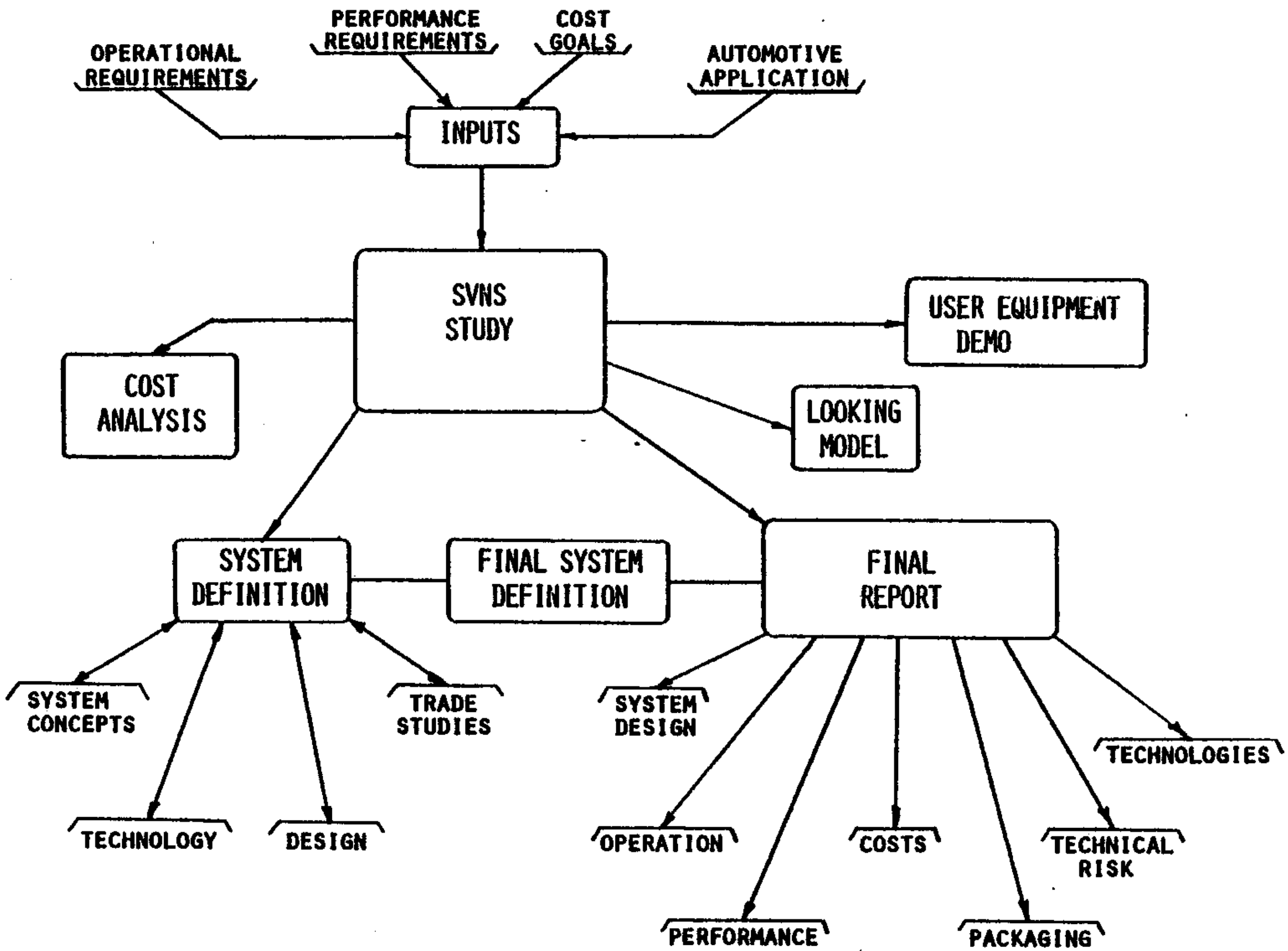
STUDY OUTPUT

A REPORT WHICH DOCUMENTS IN AS MUCH DETAIL AS NECESSARY:

1) OVERALL SYSTEM ARCHITECTURE
2) SYSTEM OPERATIONAL PROCEDURES AND CONCEPTS
3) PACKAGING CONCEPTS
4) DEVICE AND DISPLAY TECHNOLOGIES
5) TECHNICAL RISK AREAS
6) ESTIMATED MANUFACTURING COST
7) COST RISK AREAS
8) ESTIMATED DEVELOPMENT COSTS

A. SYSTEM DEFINITION
B. TECHNOLOGY
C. COST
D. RISK
E. FINAL REPORT

STUDY OVERVIEW



MINIMUM-COST DESIGN

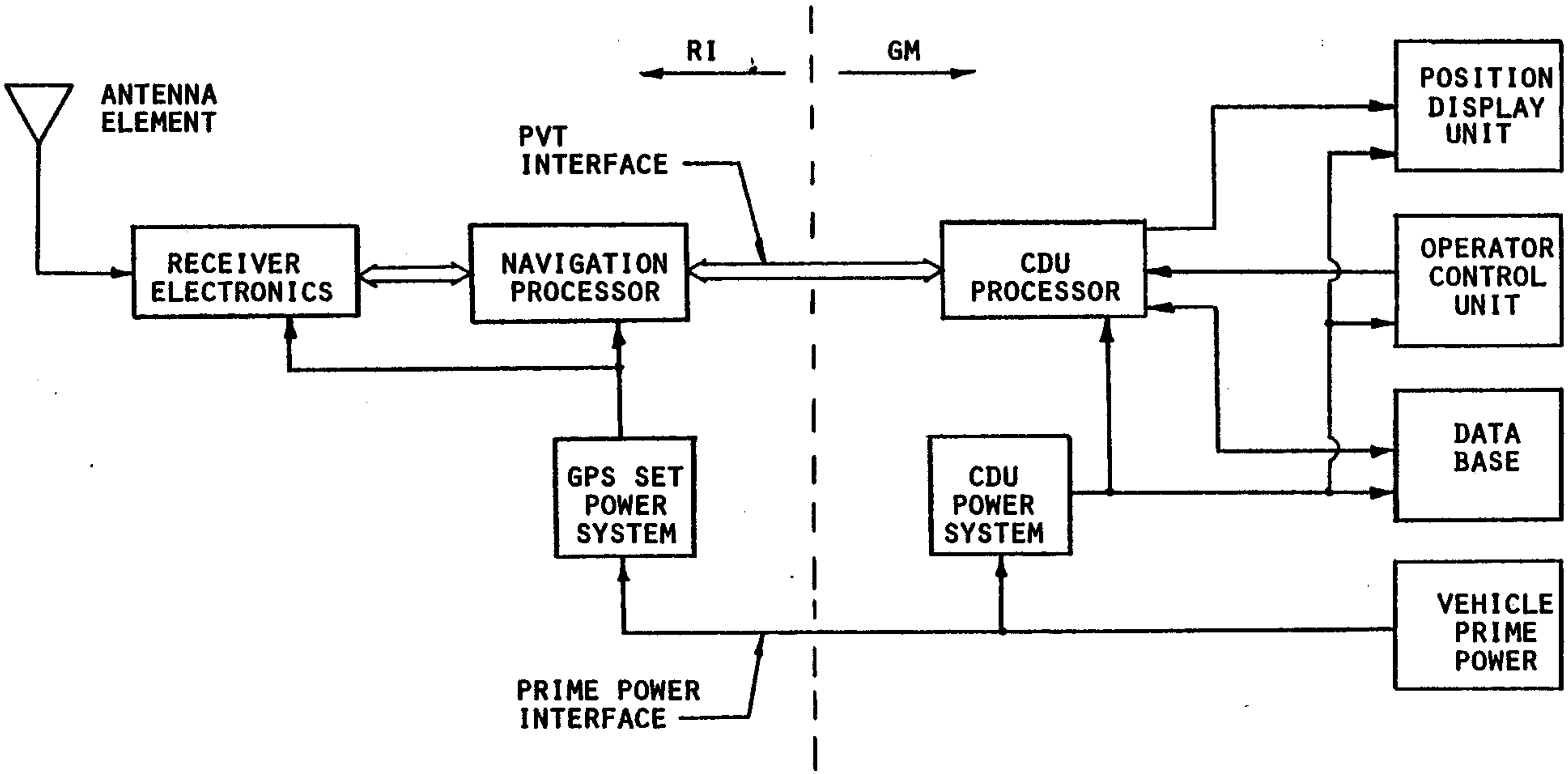
- A HIGHLY ITERATIVE PROCESS INVOLVING MANY COST VS PERFORMANCE TRADE-OFF STUDIES
- COMPLETE CHARACTERIZATION OF MOST PROMISING CANDIDATE DESIGNS
- SUMMARY OF DESIGNS
  - COST
  - PERFORMANCE
  - RISK
  - SIZE
  - WEIGHT
  - POWER
- CUSTOMER SELECTION OF "BEST" DESIGN

MINIMUM-COST DESIGN APPROACH

- DEFINE SYSTEM CONCEPT
- DEVELOP SEVERAL CANDIDATE FUNCTIONAL DESIGNS
- IDENTIFY COSTLY FUNCTIONS
- CHOOSE A BASELINE DESIGN FOR COMPLETE EVALUATION
    - BASELINE DEFINITION
    - SYSTEM LEVEL ENGINEERING REVIEW
    - LOW-COST DESIGN CYCLE
    - RISK ASSESSMENT
    - FINAL DEFINITION
- REVIEW BASELINE DESIGN FOR PRODUCT FEASIBILITY
- CHOOSE AN ALTERNATE FUNCTIONAL DESIGN FOR COMPLETE EVALUATION
- SUMMARIZE ALL PROMISING DESIGNS
- SELECT "BEST" DESIGN

MINIMUM-COST DESIGN APPROACH

SVNS SYSTEM CONCEPT



BASELINE DESIGN CONSIDERATIONS

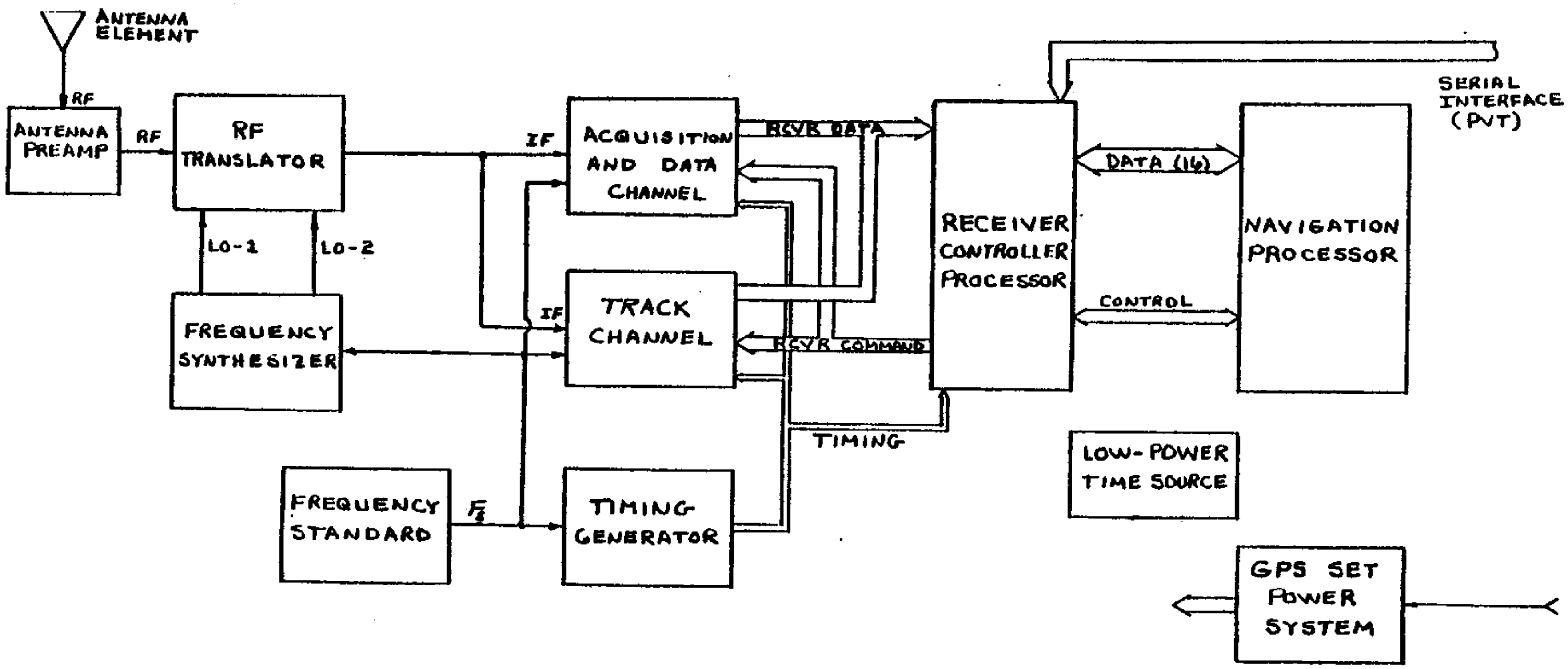
MANPACK

- L1 AND L2
  - L1-L2 4x2 SWITCH
  - IONOSPHERIC CORRECTION
  - 10 MHZ CODE GEN
- C/A AND P CODES
  - COMPLEX HARDWARE SLEW CIRCUITS
  - WIDEBAND IF
- HIGH ANTI-JAM
  - PROMPT CHANNEL
  - DELAY-LOCK TRACKING
  - T-CODE PREVENTS JAMMER FEEDTHRU
  - 2 CODE MULTIPLIERS
  - FAST AGC
- HIGH ACCURACY
  - CARRIER PHASE TRACK
  - SLOW SEQUENCE
- HIGH STABILITY FREQ STD
- RADIATION HARDENING

SVNS

- L1 ONLY
  - NO SWITCH
  - NO CORRECTION
  - 1 MHZ CODE GEN
- C/A ONLY
  - NO SLEWING
  - NARROWBAND IF
- NO HOSTILE JAMMING
  - NO PROMPT CHANNEL
  - TAU-DITHER TRACKING
  - NO T-CODE
  - ONE CODE MULTIPLIER
  - NO PULSE JAMMING
- MODERATE ACCURACY
  - CARRIER FREQUENCY TRACK
  - FAST SEQUENCE
- MIN DESIGN FREQ STD
- NO RADIATION HARDENING

BASELINE FUNCTIONAL BLOCK DIAGRAM



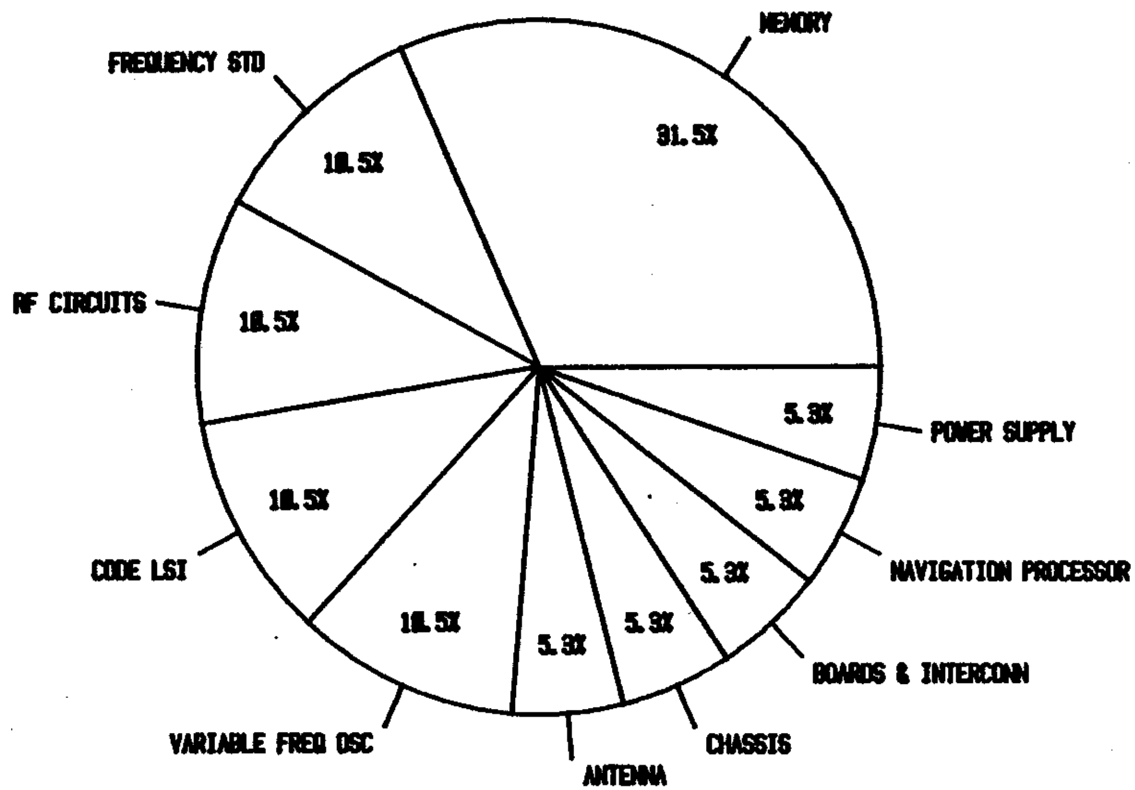
SYSTEM LEVEL ENGINEERING REVIEW

- VERIFY ADHERENCE TO SYSTEM CONCEPT
- TEST VALIDITY OF BASELINE DESIGN
- PROBE FOR MAJOR DESIGN FLAWS
- RECOMMENDATION OF FUNCTIONAL CHANGES
- "GO AHEAD" FOR LOW-COST DESIGN CYCLE

LOW-COST DESIGN CYCLE

MAJOR HARDWARE COST ELEMENTS

- FREQUENCY STANDARD
- VARIABLE FREQUENCY OSC
- CODE LSI
- RF CIRCUITS
- POWER SUPPLY
- NAVIGATION PROCESSOR
- MEMORY
- BOARDS & INTERCONNECT
- CHASSIS
- ANTENNA



COST AND PERFORMANCE TRADE-OFF STUDIES

- PRESENT
  - ANTENNA
  - FREQUENCY STANDARD
  - VARIABLE FREQUENCY OSCILLATORS
  - FREQUENCY PLAN
  - DATA DEMODULATOR
- FUTURE
  - CUSTOM LSI
  - MEMORY DENSITY, TECHNOLOGY, POWER, SPEED, COST
  - NAVIGATION PROCESSOR SELECTION
  - SINGLE OR DUAL CHANNEL
  - MECHANICAL DESIGN
  - POWER SUPPLY

LOW-COST DESIGN CYCLE

FINAL COST DETERMINATION

- COMPLETE TRADE-OFF STUDIES
- COMPLETE BASELINE MECHANICAL DESIGN
- REPLACE LOW-VOLUME ESTIMATES WITH HIGH-VOLUME MANUFACTURING

RISK AREAS

- MEMORY COST
- CUSTOM LSI COST & PERFORMANCE
- FREQUENCY STANDARD STABILITY
- μP THRUPUT
- ONE-BIT CODE POSITION DETECTOR
- ANTENNA COST

BASELINE FINAL DEFINITION

- DEPENDENT UPON:
  - COMPLETION OF LOW-COST DESIGN CYCLE
  - HIGH VOLUME PARTS AND PRODUCTION COST ESTIMATES
  - RISK ASSESSMENT

BASELINE FINAL REVIEW

- ENGINEERING REVIEW OF FINAL DESIGN
- CUSTOMER REVIEW OF COST AND DESIGN
- DETERMINE ACCEPTABILITY OF COST, PERFORMANCE, AND DESIGN
- SPECIFY NEW COST, PERFORMANCE, AND DESIGN GOALS AS DEVIATIONS FROM BASELINE
- REVIEW ALTERNATE FUNCTIONAL DESIGNS AND ASSESS PROBABILITIES OF MEETING NEW GOALS

ALTERNATE FUNCTIONAL DESIGN CHOICES

- DIGITAL CORRELATOR
- SINGLE CHANNEL SEQUENTIAL
- NONVOLATILE ELECTRONICALLY ERASABLE PROM
- LOW-POWER PROCESSOR
- SAW RESONATOR OSCILLATOR
- DIRECT CONVERSION RECEIVER
- MULTIPLEXED CODE GENERATOR
- POWER SUPPLY

COST PREDICTIONS

PRESENT CONFIDENCE LEVEL	CONFIDENCE GOAL	GPS SENSOR COST
99%	--	$12K
95%	--	5K
80%	99%	3K
50%	95%	2K
30%	80%	1K
5%	50%	.5K

MOST PROBABLE
COST RANGE
$1K - 3K

TECHNICAL SUMMARY

- MINIMUM-COST DESIGN APPROACH YIELDS BEST COST VS PERFORMANCE TRADE-OFF
- MOST PROBABLE COST RANGE FOR THE GPS SENSOR IS $1K - 3K
- BASELINE DESIGN NOW IN LOW-COST DESIGN CYCLE
- ALTERNATE FUNCTIONAL DESIGNS COMPROMISE PERFORMANCE FOR LOWER COST
- ACTUAL COST ESTIMATE REQUIRES GM ASSISTANCE IN LEARNING HIGH-VOLUME PARTS COSTS AND PRODUCTION TECHNIQUES

III. ENGINEERING DESIGN REVIEW

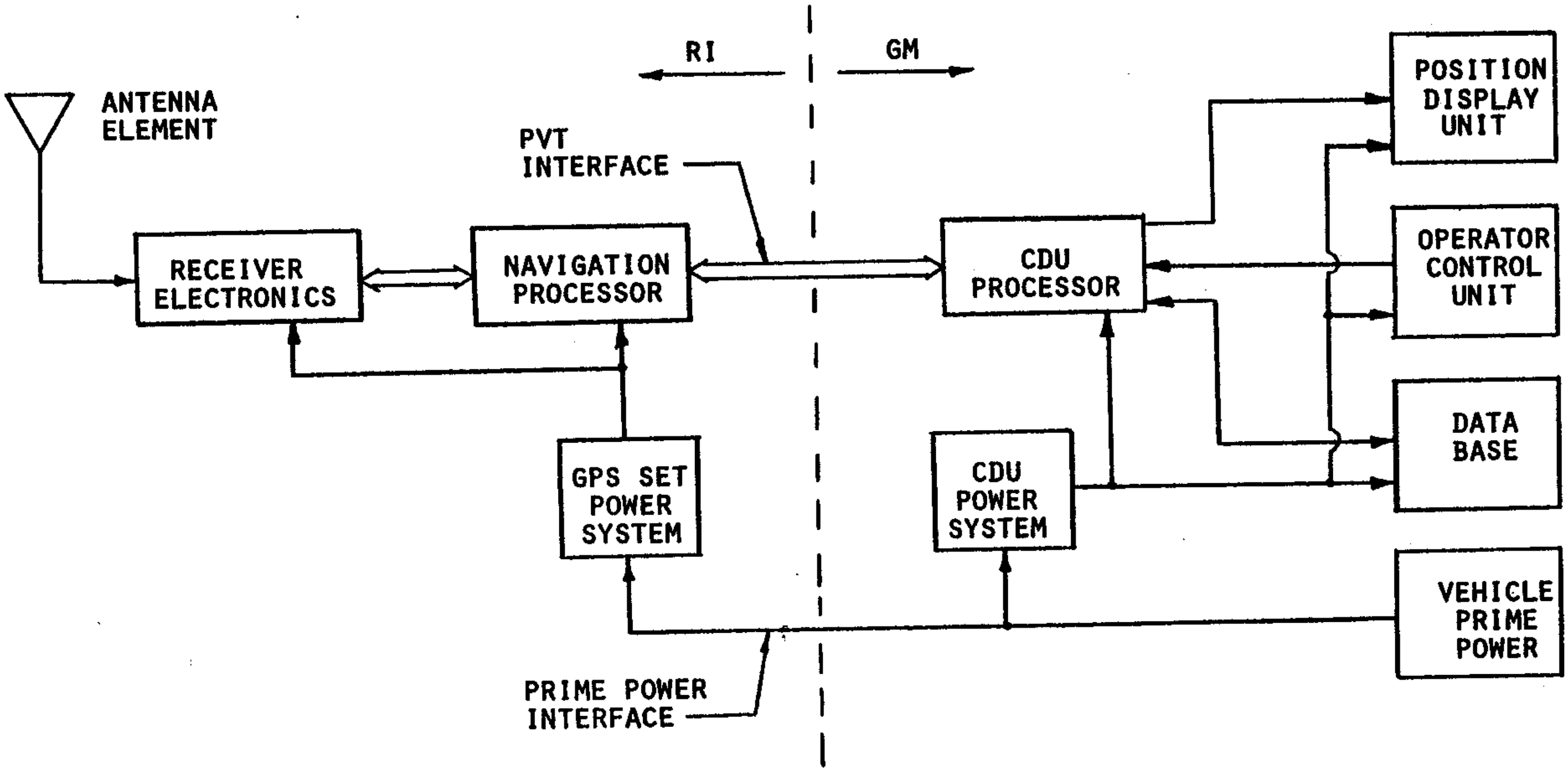
ENGINEERING DESIGN REVIEW

AGENDA

- SVNS SYSTEM CONCEPT
- MINIMUM-COST DESIGN APPROACH
- BASELINE DEFINITION
  - DESIGN CONSIDERATIONS
  - FUNCTIONAL BLOCK DIAGRAM
  - DETAILED RECEIVER BLOCK DIAGRAM
- SYSTEM LEVEL ENGINEERING REVIEW
- MAJOR HARDWARE COST ELEMENTS
- ENVIRONMENTAL REQUIREMENTS
- COST AND PERFORMANCE TRADE-OFF STUDIES
  - PRECISION FREQUENCY STANDARD
  - VCXO AND DIGITAL CARRIER VFO DESIGNS
  - ANTENNA ELEMENT DESIGNS
  - POWER SUPPLY
- COST ANALYSIS
  - COST ESTIMATING
  - HARDWARE DESIGN EXAMPLE
- CUSTOM LSI DESIGN
  - CANDIDATES
  - TRADE-OFFS
  - CODE GENERATOR LOGIC
  - CHIP SIZE COMPARISONS
  - LSI PARTITIONING
  - DIGITAL CARRIER VFO
- PRELIMINARY SIZE AND POWER ESTIMATES
- FINAL COST DETERMINATION
- RISK AREAS
- BASELINE DESIGN COMPLETION
- ALTERNATE FUNCTIONAL DESIGN CHOICES
- TECHNICAL SUMMARY
- FINAL REPORT OUTLINE

MINIMUM-COST DESIGN APPROACH

SVNS SYSTEM CONCEPT



DESIGN-TO-COST APPROACH

- DEVELOP A BASELINE SYSTEM
  - ELECTRICAL, INTERCONNECT, CHASSIS
  - REASONABLE COST AND RISK
  - MEET MOST PERFORMANCE* GOALS
- PERFORM TRADE-OFF STUDIES
  - COST
  - RISK
  - PERFORMANCE*

  FIND THE "KNEE OF THE CURVE"
- CHOOSE MINIMUM COST ALTERNATIVES THAT MEET ACCEPTABLE PERFORMANCE* AND RISK
- UPDATE BASELINE
  - ELECTRICAL, INTERCONNECT, CHASSIS
  - COST AND RISK
  - PERFORMANCE*
- EVALUATE NEW SYSTEM FOR OVERALL FEATURES
- ITERATE UNTIL DESIGN HAS CUSTOMER APPROVAL

* IT IS DIFFICULT TO ASSESS COST VS TECHNICAL PERFORMANCE

BASELINE DESIGN CONSIDERATIONS

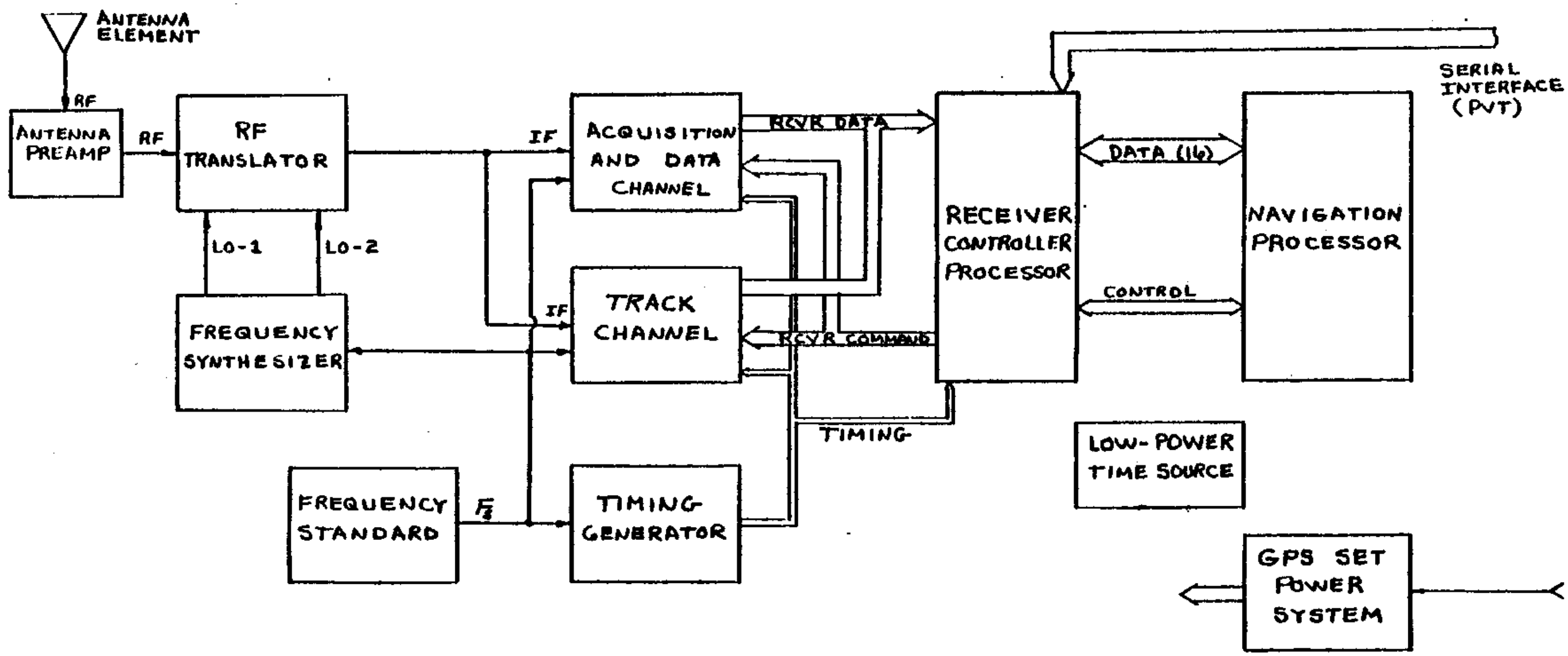
MANPACK

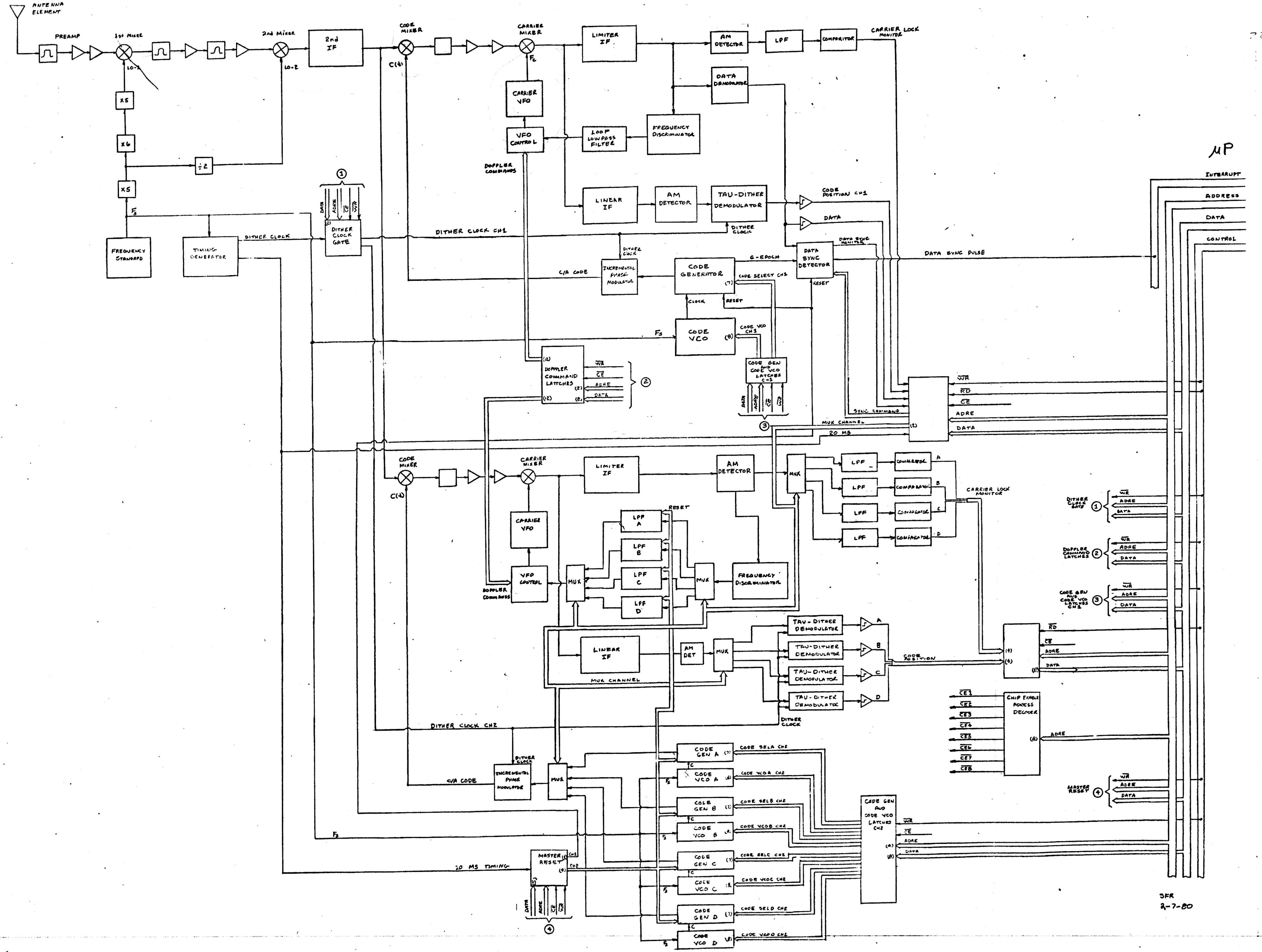
- L1 AND L2
  - L1-L2 4x2 SWITCH
  - IONOSPHERIC CORRECTION
  - 10 MHZ CODE GEN
- C/A AND P CODES
  - COMPLEX HARDWARE SLEW CIRCUITS
  - WIDEBAND IF
- HIGH ANTI-JAM
  - PROMPT CHANNEL
  - DELAY-LOCK TRACKING
  - T-CODE PREVENTS JAMMER FEEDTHRU
  - 2 CODE MULTIPLIERS
  - FAST AGC
- HIGH ACCURACY
  - CARRIER PHASE TRACK
  - SLOW SEQUENCE
- HIGH STABILITY FREQ STD
- RADIATION HARDENING

SVNS

- L1 ONLY
  - NO SWITCH
  - NO CORRECTION
  - 1 MHZ CODE GEN
- C/A ONLY
  - NO SLEWING
  - NARROWBAND IF
- NO HOSTILE JAMMING
  - NO PROMPT CHANNEL
  - TAU-DITHER TRACKING
  - NO T-CODE
  - ONE CODE MULTIPLIER
  - NO PULSE JAMMING
- MODERATE ACCURACY
  - CARRIER FREQUENCY TRACK
  - FAST SEQUENCE
- MIN DESIGN FREQ STD
- NO RADIATION HARDENING

BASELINE FUNCTIONAL BLOCK DIAGRAM





ANTENNA ELEMENT
PREAMP
1st MIXER
2nd MIXER
LO-1
LO-2
2nd IF
CODE MIXER
CARRIER MIXER
LIMITER IF
AM DETECTOR
LPF
COMPARITOR
CARRIER LOCK MONITOR
DATA DEMODULATOR
CARRIER VFO
VFO CONTROL
LOOP LOWPASS FILTER
FREQUENCY DISCRIMINATOR
x5
x6
÷2
DOPPLER COMMANDS
LINEAR IF
AM DETECTOR
TAU-DITHER DEMODULATOR
CODE POSITION CH1
DATA
DITHER CLOCK
FREQUENCY STANDARD
TIMING GENERATOR
DITHER CLOCK
DITHER CLOCK GATE
DITHER CLOCK CH1
INCREMENTAL PHASE MODULATOR
C/A CODE
CODE GENERATOR
G-EPOCH
DATA SYNC DETECTOR
DATA SYNC PULSE
CODE SELECT CH1
CLOCK
RESET
CODE VCO
CODE VCO CH1
DOPPLER COMMAND LATCHES
CODE GEN AND CODE VCO LATCHES CH1
μP
INTERRUPT
ADDRESS
DATA
CONTROL
WR
RD
CE
ADRE
DATA
SYNC COMMAND
MUX CHANNEL
20 MS
MUX
COMPARATOR
CARRIER LOCK MONITOR
LPF A
LPF B
LPF C
LPF D
RESET
MUX CHANNEL
AM DET
TAU-DITHER DEMODULATOR
CODE POSITION
DITHER CLOCK
DITHER CLOCK GATE
DOPPLER COMMAND LATCHES
CODE GEN AND CODE VCO LATCHES CH2
CHIP ENABLE ADRESS DECODER
CE1
CE2
CE3
CE4
CE5
CE6
CE7
CE8
MASTER RESET
DITHER CLOCK CH2
CODE GEN A
CODE VCO A
CODE GEN B
CODE VCO B
CODE GEN C
CODE VCO C
CODE GEN D
CODE VCO D
CODE SELA CH2
CODE VCOA CH2
CODE SELB CH2
CODE VCOB CH2
CODE SELC CH2
CODE VCOC CH2
CODE SELD CH2
CODE VCOD CH2
20 MS TIMING
SFR
2-7-80

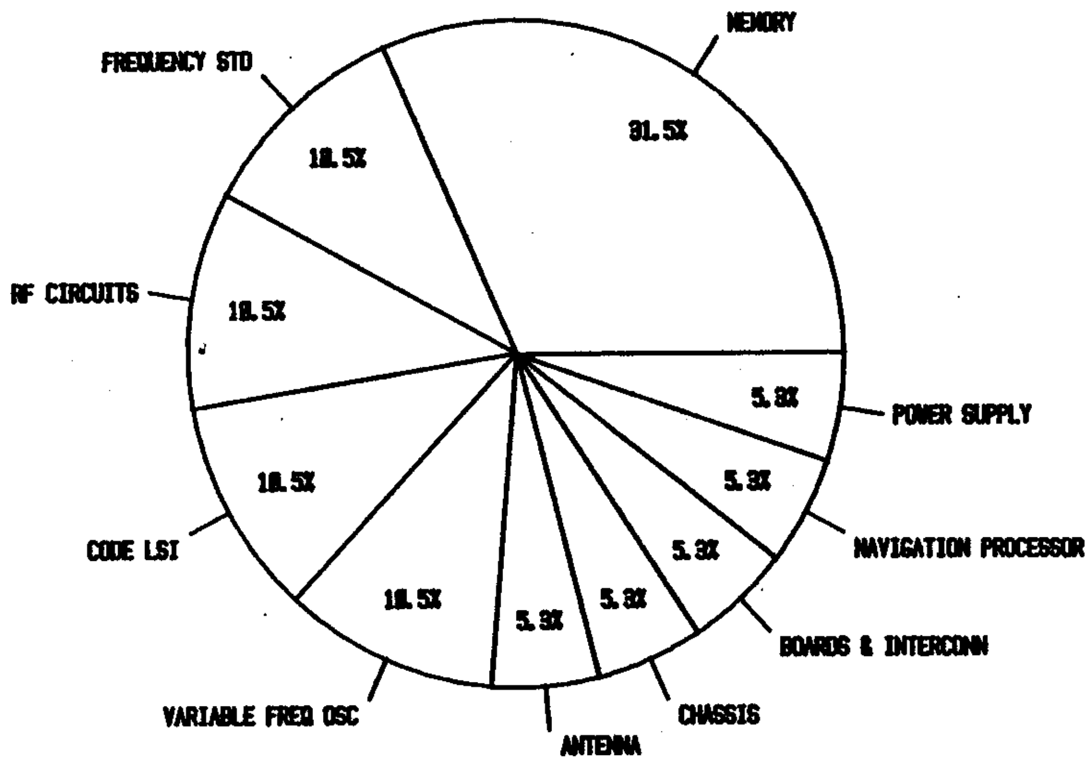
SYSTEM LEVEL ENGINEERING REVIEW

- REVIEW IS COMPLETE
- PRESENT BASELINE SATISFIES SYSTEM CONCEPT
- ALL FUNCTIONS IN BASELINE ARE FEASIBLE
  - DATA DEMOD IS A NOVEL DESIGN BUT TECHNICALLY VALID
  - MULTIPLE CODE VCO OBVIATES SEVERE RESET LOGIC PROBLEM
  - DUAL CHANNELS ALLOW CONTINUOUS TRACKING
  - TWO PROCESSOR CONCEPT ALLOWS LOWER SPEEDS
  - FREQUENCY TRACKING SIMPLIFIES HARDWARE
- NO DESIGN FLAWS FOUND
- LOW-COST DESIGN CYCLE EFFORT APPROVED

LOW-COST DESIGN CYCLE

MAJOR HARDWARE COST ELEMENTS

- FREQUENCY STANDARD
- VARIABLE FREQUENCY OSC
- CODE LSI
- RF CIRCUITS
- POWER SUPPLY
- NAVIGATION PROCESSOR
- MEMORY
- BOARDS & INTERCONNECT
- CHASSIS
- ANTENNA



ENVIRONMENTAL CONSIDERATIONS FOR TRUNK MOUNTED

SVNS RECEIVER

ENVIRONMENTAL REQUIREMENT	GM ENVIRONMENTAL SPECIFICATION	REMARKS
Temperature	3.5, 3.6	$-40^{o}C$ to $+85^{o}C$ extremes, must pass thermal shock test
Humidity	4.	98% @ $38^{o}C$, 80% @ $66^{o}C$, frost
Immersion	N.A.	Standing water on floor possible
Shock	6.	48" drop test seems quite severe for sophisticated electronics
Vibration	7.1 - 7.5	Resonance dwells until fatigue failure, 10^6 cycles, or eight hours, whichever occurs first. Seems severe
Salt Spray	N.A.	A standing saturated salt solution is possible on the floor
Sand & Dust	N.A.	A heavy build-up of sand and dust is probable
Oils & Chemicals	N.A.	Spillage of all chemicals listed in SAE J1211, Section 4.4 is possible

NOTE: All tests are described in GM document "Environmental Specification for Electronic Systems", dated 6-13-73.

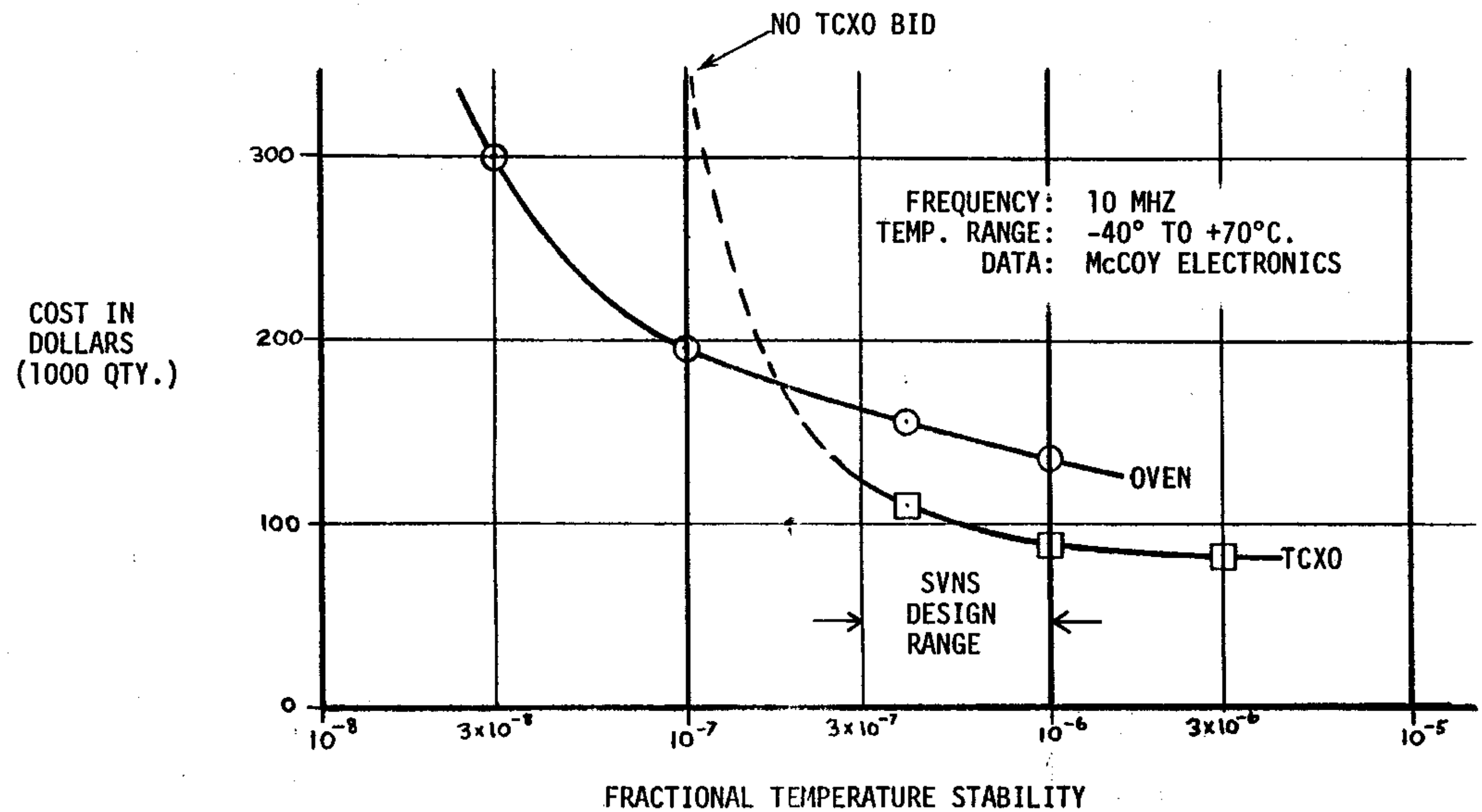
COST AND PERFORMANCE TRADE-OFF STUDIES

	STUDY	STATUS
1.	FREQUENCY STANDARD	COMPLETE
2.	CARRIER VFO	COMPLETE EXCEPT COST AND RISK
3.	FREQUENCY PLAN	COMPLETE EXCEPT SPURIOUS ANALYSIS
4.	CODE VCO	COMPLETE
5.	CUSTOM LSI	STARTED
6.	ANTENNA	COMPLETE EXCEPT COST
7.	POWER SUPPLY	STARTED
8.	DATA DEMODULATOR	COMPLETE
9.	MEMORY SELECTION	STARTED (NMOS CANDIDATE)
10.	PROCESSOR SELECTION	STARTED (8086 CANDIDATE)
11.	SINGLE VS DUAL CHANNEL	NOT STARTED
12.	MECHANICAL DESIGN	CANDIDATES AND ALTERNATIVES IDENTIFIED

FREQUENCY STANDARD TRADE-OFFS

- LARGE FREQUENCY VARIATIONS WITH TEMPERATURE CAUSE LONG ACQUISITION TIMES.
- TEMPERATURE STABILITY IS DRIVING FACTOR IN COST.
- OVENIZED OSCILLATOR REQUIRES HIGH POWER (3-6W) AND LONG WARM-UP TIME (5-10 MIN.).
- TCXO REQUIRES LITTLE POWER (200 MW) AND HAS QUICK WARM-UP (10 SEC.).
- CAN SUFFICIENT STABILITY BE OBTAINED AT LOW COST?
- CAN TCXO BE USED?

FREQUENCY STANDARD COST VS. STABILITY



FREQUENCY STANDARD TRADE-OFF RESULTS

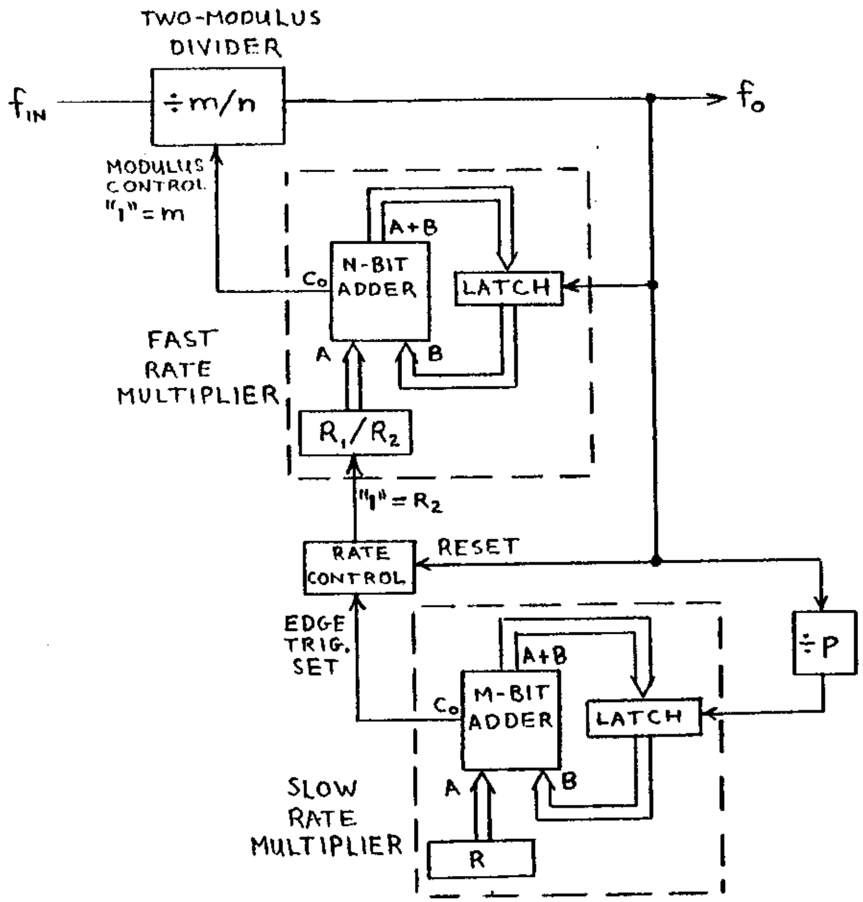
- BASELINE TARGET - 1 PPM TCXO.
  - LOW COST, PAST "KNEE" OF CURVE
  - ACQUISITION TIME NOT EXCESSIVE
- ONLY RELATIVE COSTS AVAILABLE.
- COST FOR HIGH-VOLUME AUTOMATED PRODUCTION NOT KNOWN.

VCXO AND DIGITAL
CARRIER VFO DESIGNS

CARRIER VFO TRADE-OFFS

- CARRIER MUST BE TRACKED BY PLL OR AFC.
- DIGITAL VFO (RATE MULTIPLIER VFO) VS. VCXO.
- WHAT IMPACT DOES EACH HAVE ON FREQUENCY PLAN?
- WHAT IS INVOLVED IN VFO CONTROL CIRCUITRY?
- HOW DOES VCXO "SETABILITY" IMPACT COST?
- WHAT IS COST FOR EACH?

DIGITAL FREQUENCY GENERATION



A. SINGLE RATE MULTIPLIER (ASSUME FAST RATE = R_1)

- Value in accumulator increases by R_1 on each cycle of f_o, generating R_1 carries for every 2^N cycles of f_o.
- When carry occurs, modulus is changed to m.
- In 2^N cycles of f_o there will be R_1 counts of m and (2^N-R_1) counts of n, yielding an average count of:

$$\bar{c} = \frac{R_1 m + (2^N - R_1)n}{2^N} = \frac{R_1}{2^N}(m - n) + n$$

- The average count will be between n and m.

B. DUAL RATE MULTIPLIER

- Slow rate multiplier increments once every P cycles of f_o and generates R carries every $2^M p$ cycles of f_o.
- When slow accumulator generates a carry, fast rate changes to R_2 on a "one-shot" basis.
- As a result, fast rate multiplier will generate slightly more carries if R_2 is larger than R_1, and less if R_2 is smaller than R_1.
- The average count for the dual rate multiplier can be shown to be:

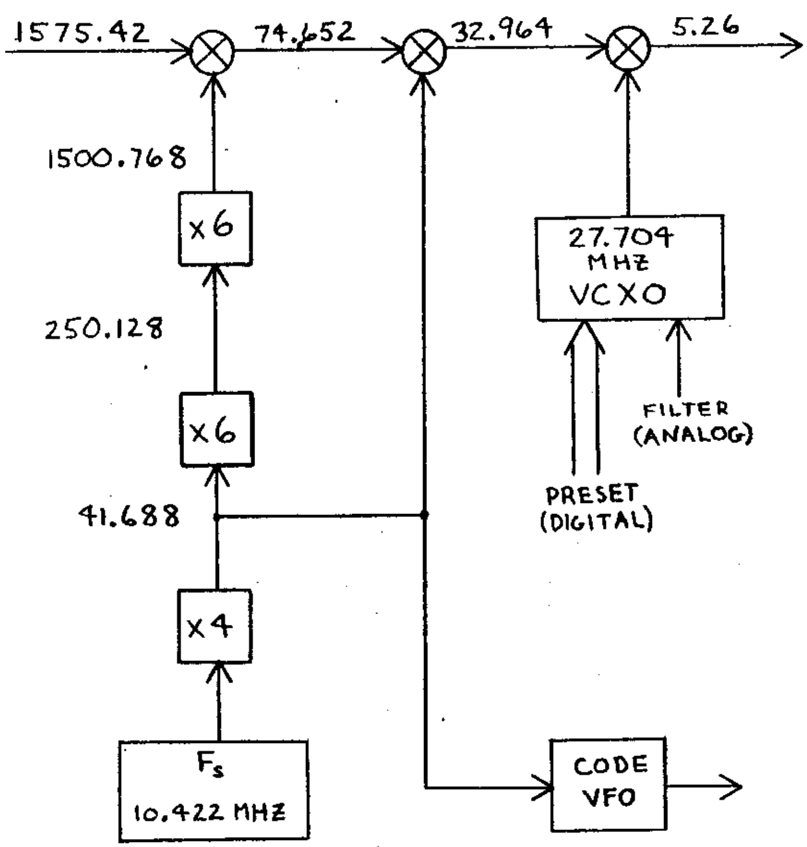
$$\bar{c} = n + \frac{R_1}{2^N}(m - n) + \frac{R}{2^M}\frac{(R_2 - R_1)(m - n)}{2^N p}$$

VCXO AND DIGITAL VFO PERFORMANCE CONTRASTS

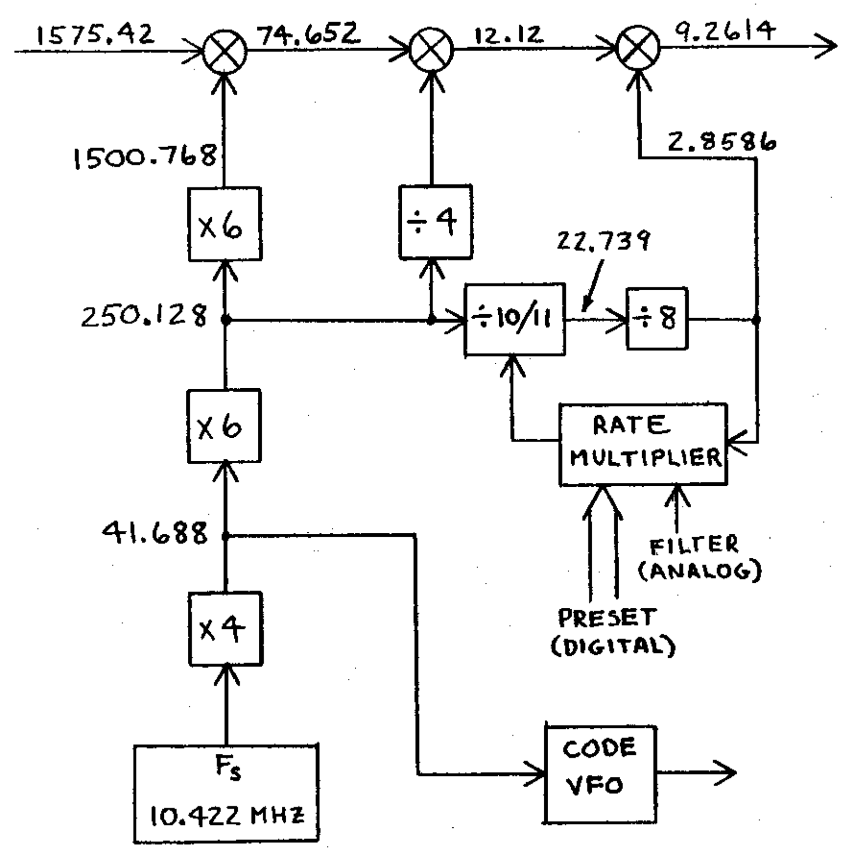
	VCXO	DIGITAL VFO
LINEARITY	DIFFICULT TO OBTAIN	ANALYTICALLY PREDICTABLE NON-LINEARITY
STABILITY	DIFFICULT TO OBTAIN	DETERMINED SOLELY BY REFERENCE
DIGITAL PRESET	REQUIRES HIGH-ACCURACY D/A	DIRECT
ANALOG FILTER INPUT	DIRECT	REQUIRES LOW-ACCURACY A/D
SUPPLY VOLTAGE(S)	MAY REQUIRE + AND - VOLTAGE, OR + VOLTAGE GREATER THAN 10V	SINGLE +5V SUPPLY
POWER	LOW - APPR. 100 MW.	HIGH - .5 TO 1 WATT
OUTPUT FREQUENCY	CONTINUOUSLY VARIABLE	DISCRETE
SPECTRAL PURITY	SPURIOUS-FREE	MANY SPURIOUS OUTPUTS
CUSTOM LSI	NOT APPLICABLE	YES

FREQUENCY PLAN ALTERNATIVES

VCXO



DIGITAL VFO

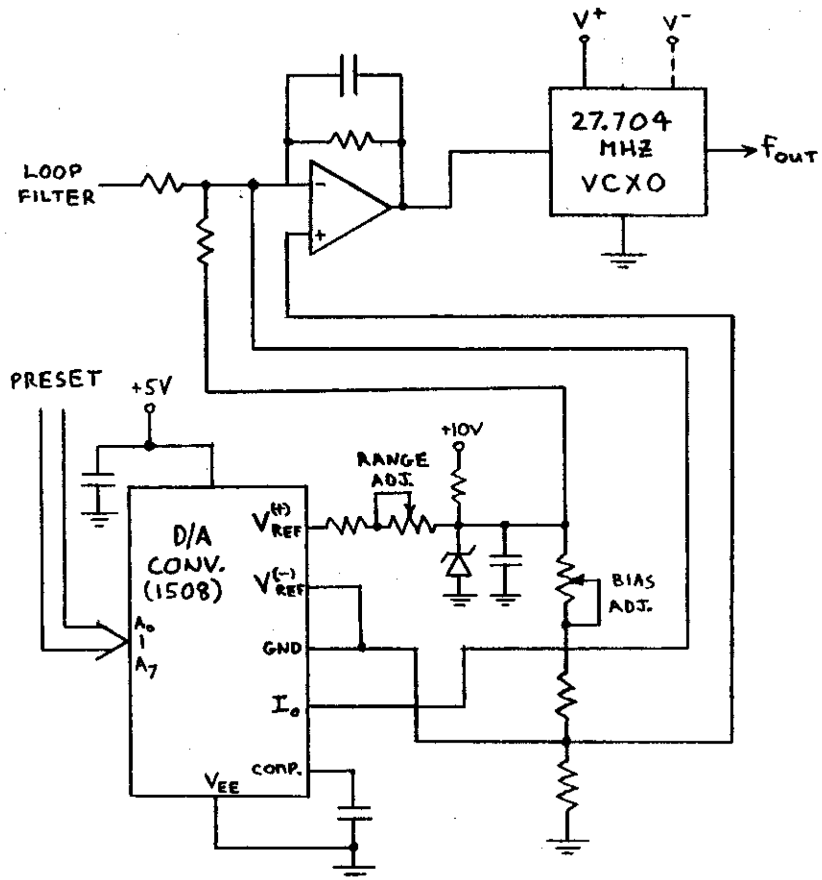


SURFACE VEHICLE NAVIGATION SYSTEM FEASIBILITY STUDY

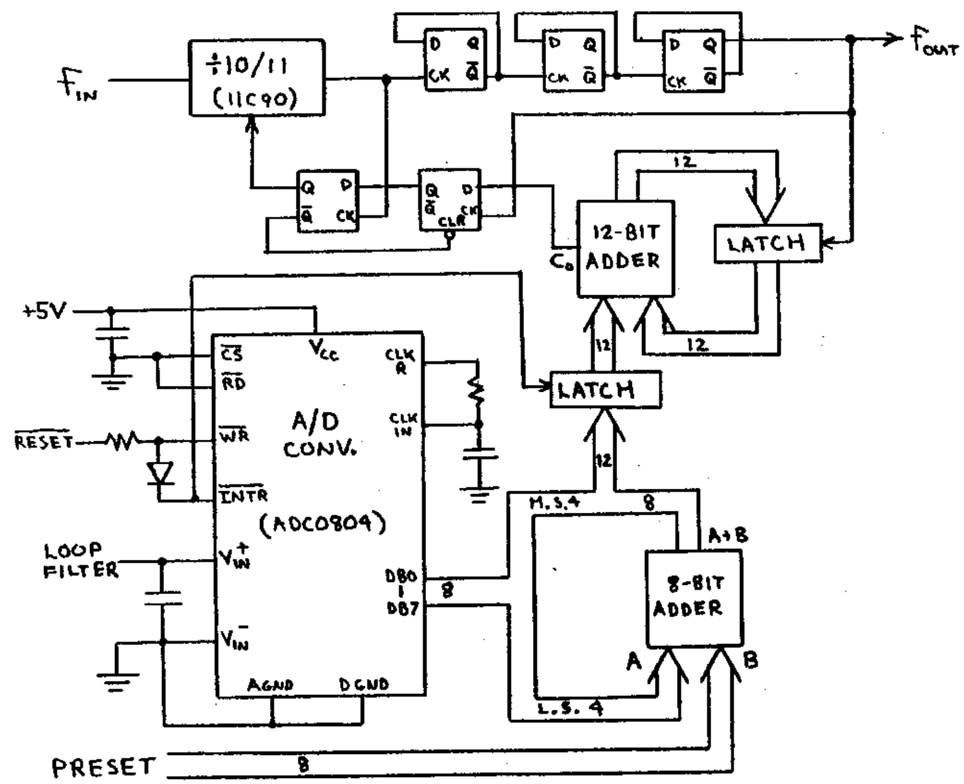
NAVSTAR GLOBAL POSITIONING SYSTEM

DIGITAL VFO VS. VCXO CIRCUITRY

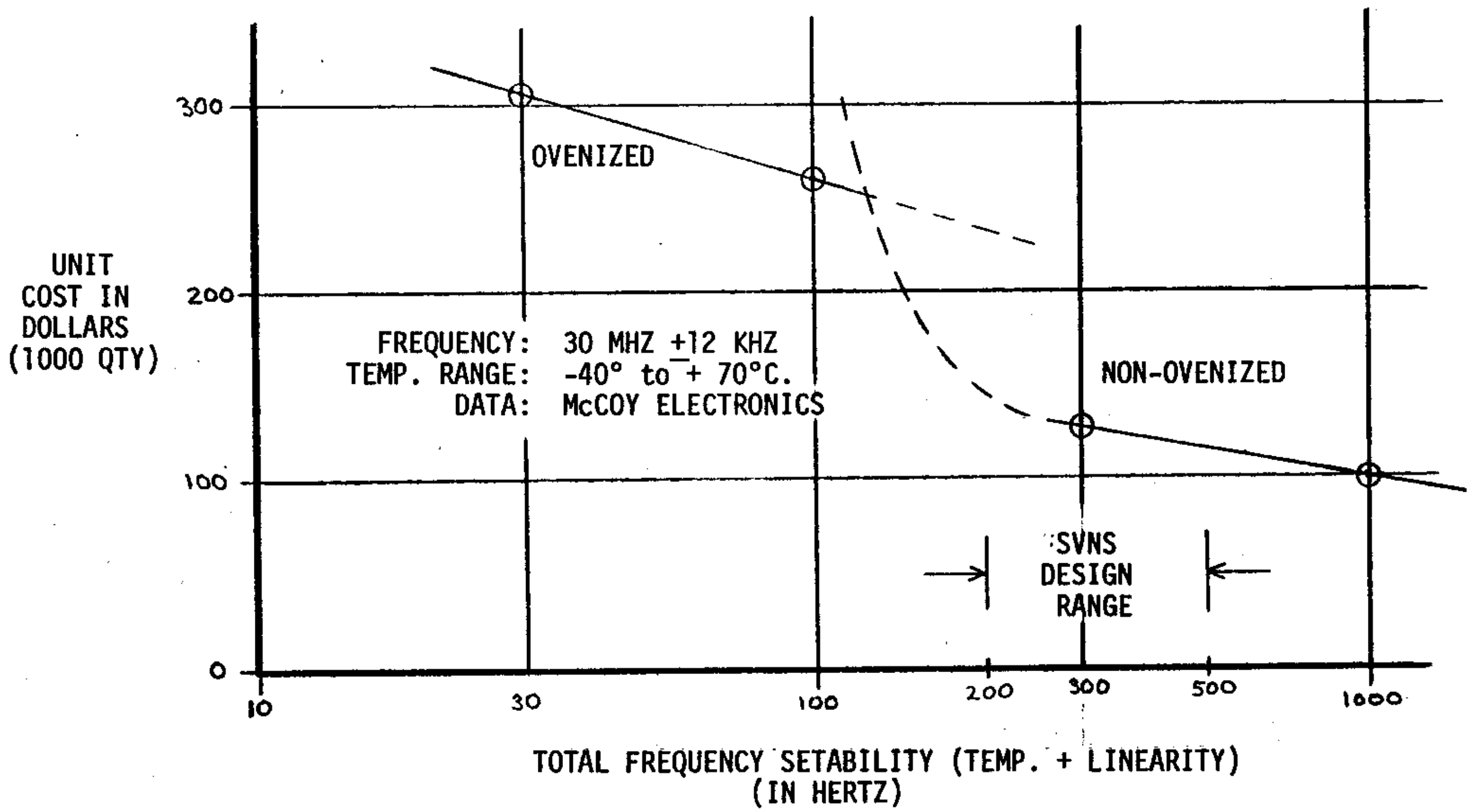
VCXO



DIGITAL VFO



VCXO COST VS. SETABILITY



CARRIER VFO TRADE-OFF RESULTS

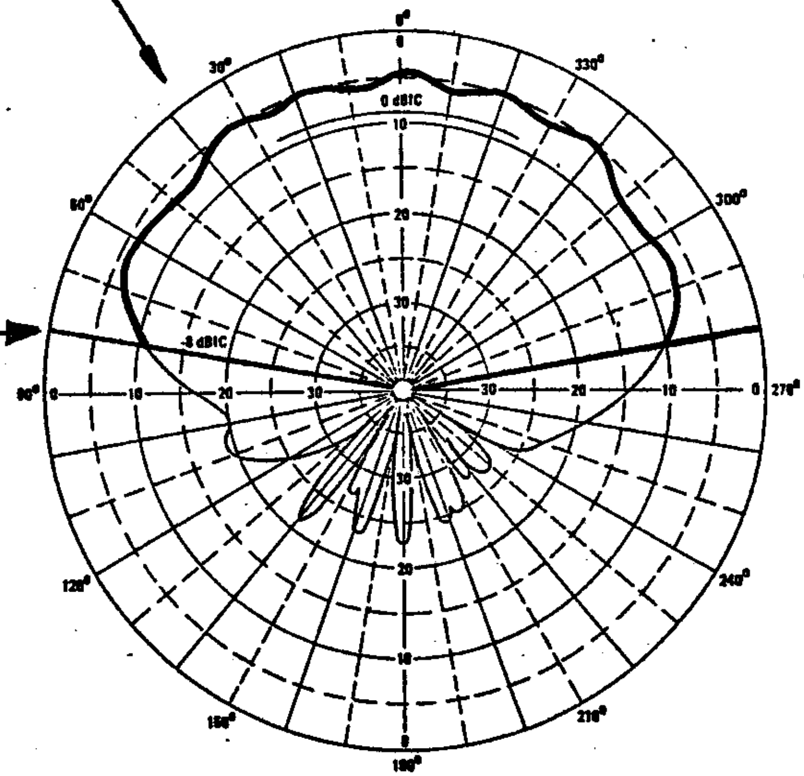
- BOTH APPROACHES ALLOW RELATIVELY SIMPLE FREQUENCY PLANS.
  - DIGITAL VFO IMPACTS SYNTHESIZER (EXTRA DIVIDE-BY-FOUR).
- VCXO SUPPORT CIRCUITRY INEXPENSIVE BUT REQUIRES ADJUSTMENT.
- NON-OVENIZED VCXO CAN PROVIDE ADEQUATE "SETABILITY".
- COST (OFF-THE-SHELF):
  - DIGITAL VFO: $15 + $6 SUPPORT = $21
  - VCXO: ? + $3 SUPPORT = ?
- FINAL DECISION WILL DEPEND UPON REALISTIC, HIGH QUANTITY VCXO COST ESTIMATE.

ANTENNA ELEMENT DESIGNS

REQUIREMENTS:
- LOW COST
- AUTOMOTIVE MOUNTING
- OMNI PATTERN
- GAIN ≥ -2 dBiC
- $NF_{SYS} \leq 5$ dB

DESIGNS:

- VERTICAL STUB
- SINGLE ELEMENT MICROSTRIP
- MICROSTRIP PATCH
- MULTI-ELEMENT MICROSTRIP
- BALL & STEM
- CONICAL SPIRAL
- VERTICAL HELIX



POWER SUPPLY

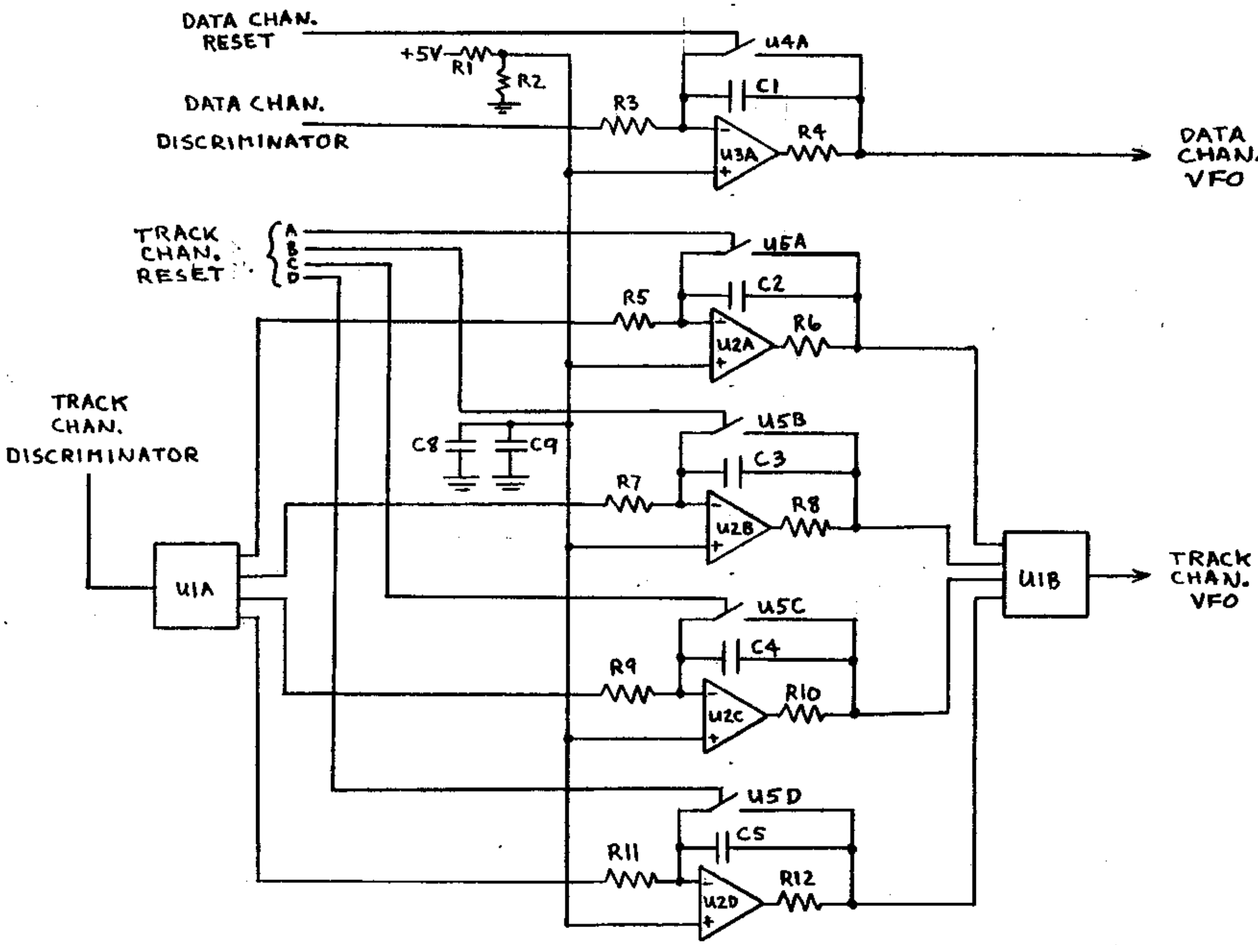
- SERIES REGULATOR
  - SIMPLE
  - LOW COST
  - POOR EFFICIENCY
  - SINGLE POLARITY ONLY
  - RESTRICTS DESIGN FREEDOM
  - LIMITED ISOLATION
- SWITCHING REGULATOR
  - MORE COMPLEX
  - HIGHER COST
  - GOOD EFFICIENCY
  - DUAL POLARITY
  - IMPROVED DESIGN FREEDOM
  - IMPROVED ISOLATION
- CHOICE YET TO BE MADE

COST ESTIMATING

- DESIGN HARDWARE WITH STANDARD PARTS WHERE POSSIBLE.
- GENERATE PARTS LIST AND SCHEMATIC.
- ESTIMATE BOARD AREA, POWER CONSUMPTION AND COST.

HARDWARE DESIGN EXAMPLE

CARRIER LOOP FILTERS



PARTS LIST

U1	4052B DUAL MUX
U2	LM2902 QUAD OP-AMP
U3	LM2904 DUAL OP-AMP
U4,5	4016B QUAD SWITCH
R1,2	1% METAL FILM
R3-12	1/4 W, 10% CARB. COMP.
C1-8, 10-12	CERAMIC
C9	TANTALUM

CUSTOM LSI CANDIDATES

- CODE GENERATORS, LATCHES AND CONTROL.
- CODE VFO'S, LATCHES AND CONTROL.
- DIGITAL CARRIER VFO, LATCHES AND PRESET.
- TIMING GENERATOR.

CUSTOM LSI TRADE-OFFS

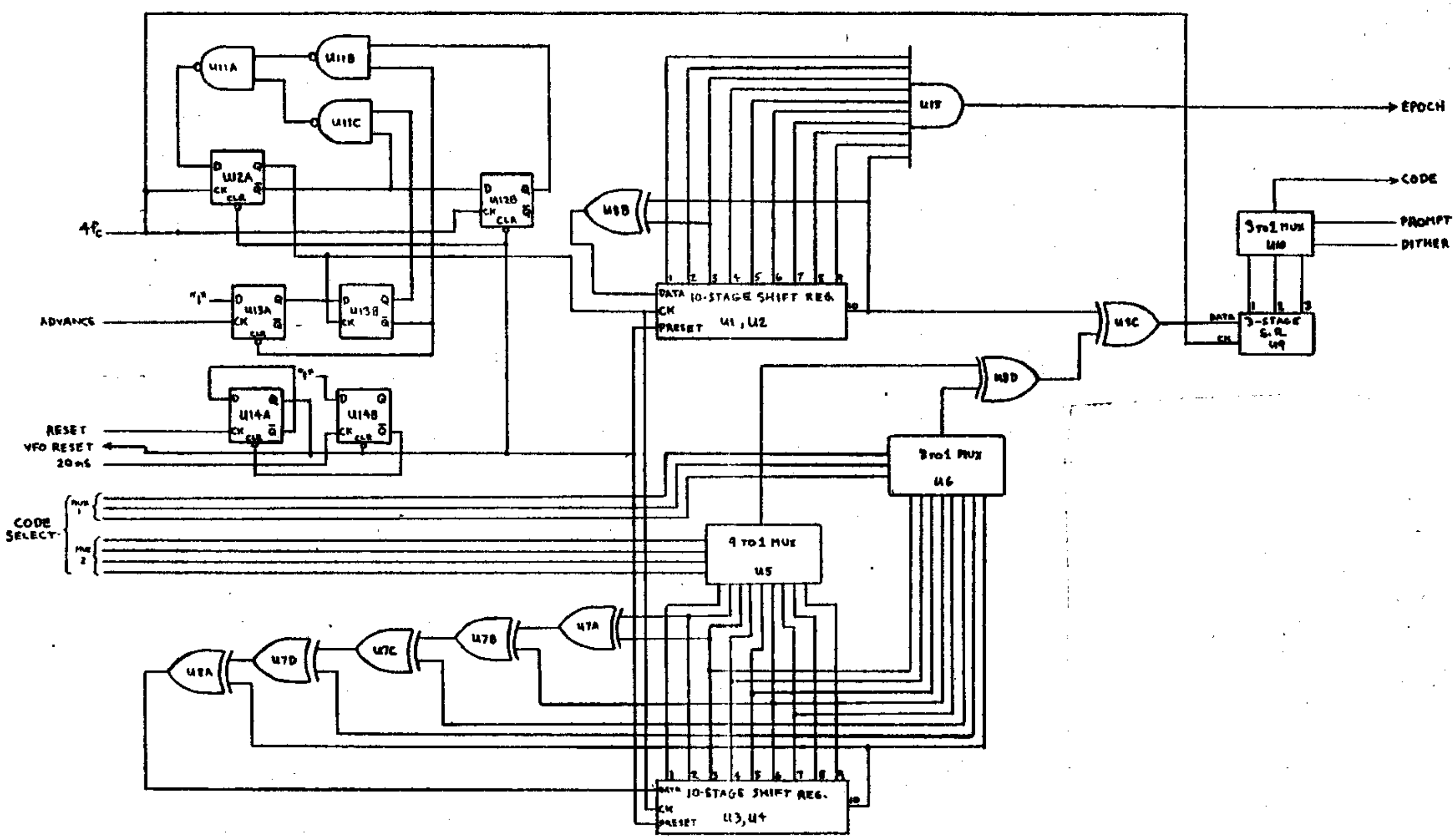
- IDENTIFY CANDIDATE FUNCTIONS.

- FUNCTIONAL DEFINITION (LOGIC DIAGRAMS).

- FUNCTIONAL PARTITIONING (INDIVIDUAL CHIP FUNCTIONS).
  - SPEED REQUIREMENTS
  - LOGIC CELL COUNT
  - CHIP SIZE

- EVALUATE PARTITIONING OPTIONS.

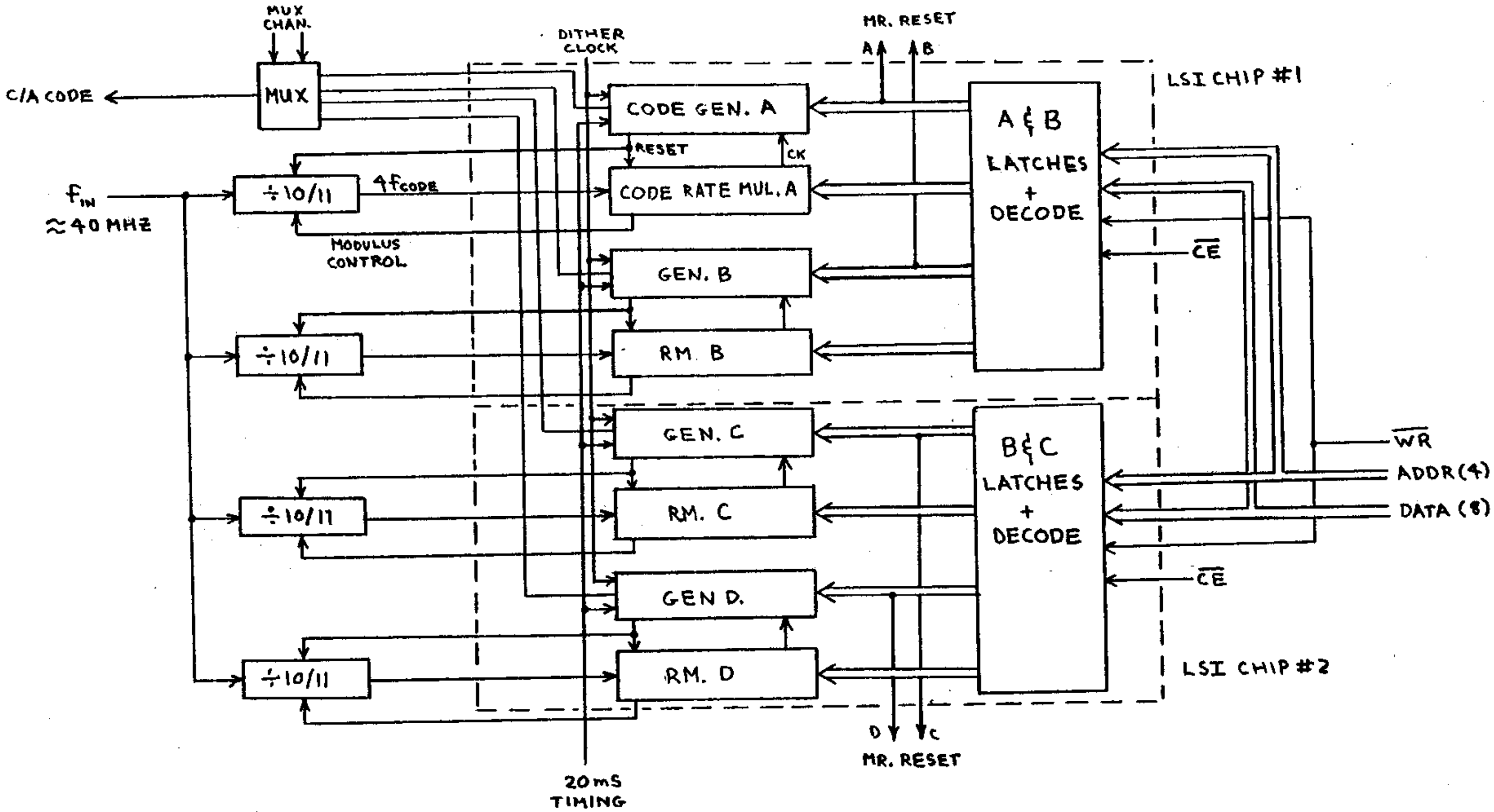
CODE GENERATOR LOGIC



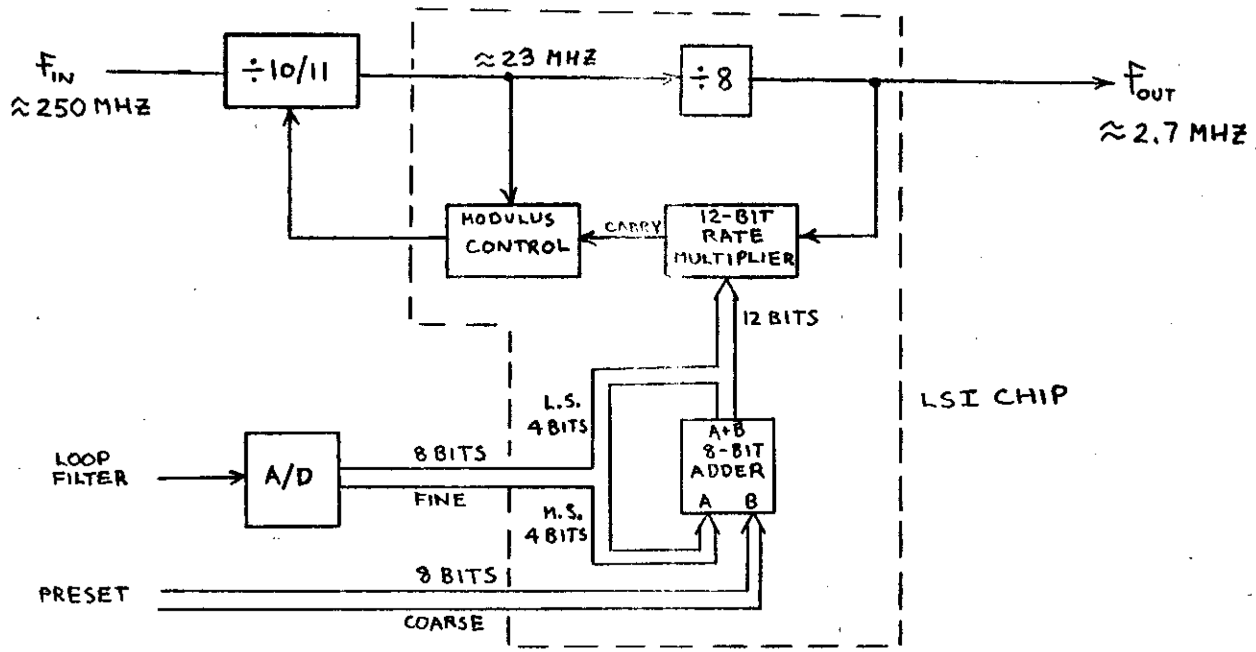
CHIP SIZE COMPARISONS

	LARGE CHIP	SMALL CHIP
• FUNCTIONAL CAPABILITIES	HIGH	LOW
• BOARD AREA REQUIREMENT	LOW	HIGH
• INTERCONNECT REQUIREMENTS	LOW	HIGH
• POWER DISSIPATION	HIGH	LOW
• YIELD (COST)	LOW (HIGH)	HIGH (LOW)

CODE LSI PARTITIONING



DIGITAL CARRIER VFO LSI



PRELIMINARY SIZE AND POWER ESTIMATES

	FUNCTION	BOARD AREA	POWER
1.	RF PREAMP	6	0.2
2.	SYNTHESIZER	9	0.5
3.	FREQ STD*	4	0.2
4.	RF TRANSLATOR	5	0.4
5.	DATA CHANNEL	30	3.0
6.	TRACK CHANNEL	30	3.0
7.	RCVR CONTROLLER	6	2.1
8.	NAV PROCESSOR	40	11.6
9.	LOW-POWER TIME SOURCE	2	-
10.	POWER SYSTEM**	15	10.5
		147 IN^2	31.5 WATTS

* TCXO, 2" x 2" x 1"

** 50% EFF, 3" x 5" x 1"

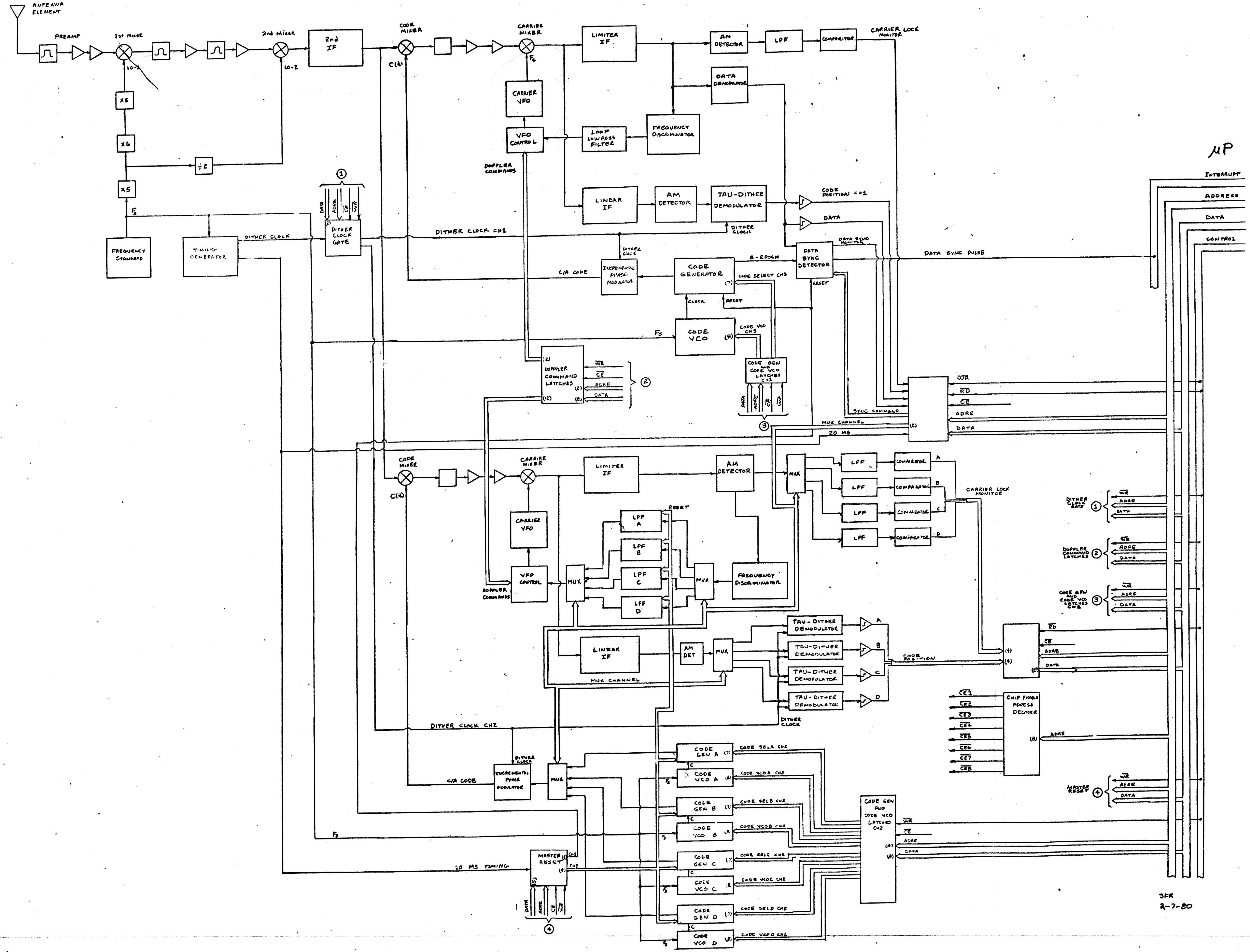
FINAL COST DETERMINATION

- ROCKWELL COST ESTIMATE BASED ON AVIONICS PRODUCTION
  - COMPLETE TRADE STUDIES
  - COMPLETE CIRCUIT DIAGRAMS
  - DEVELOP PARTS LISTS
  - DETERMINE PARTS LISTS
  - COMPLETE MECHANICAL DESIGN
  - DETERMINE MECHANICAL COSTS
  - OBTAIN FACTORY LABOR COSTS

- GM HIGH-VOLUME COST ESTIMATE REQUIRES ASSISTANCE IN
  - DETERMINING HIGH-VOLUME DESIGN TRADE-OFFS
  - AUTOMATED TEST AND CIRCUIT ADJUSTMENT
  - DETERMINING HIGH-VOLUME PARTS COST
  - AUTOMATED ASSEMBLY TECHNIQUES

RISK AREAS

- MEMORY COST
- CUSTOM LSI COST & PERFORMANCE
- FREQUENCY STANDARD STABILITY
- μP THRUPUT
- ONE-BIT CODE POSITION DETECTOR
- ANTENNA COST



ANTENNA ELEMENT
PREAMP
1st MIXER
LO-1
2nd MIXER
LO-2
2nd IF
X5
X6
÷2
X5
Fs
FREQUENCY STANDARD
TIMING GENERATOR
DITHER CLOCK
DITHER CLOCK GATE
DATA
ADRE
CE
WR
CODE MIXER
C(t)
CARRIER MIXER
Fc
CARRIER VFO
VFO CONTROL
DOPPLER COMMANDS
LIMITER IF
AM DETECTOR
LPF
COMPARITOR
CARRIER LOCK MONITOR
DATA DEMODULATOR
FREQUENCY DISCRIMINATOR
LOOP LOWPASS FILTER
LINEAR IF
AM DETECTOR
TAU-DITHER DEMODULATOR
DITHER CLOCK
CODE POSITION CH1
DATA
DITHER CLOCK CH1
INCREMENTAL PHASE MODULATOR
C/A CODE
CODE GENERATOR
G-EPOCH
DATA SYNC DETECTOR
DATA SYNC MONITOR
DATA SYNC PULSE
CODE SELECT CH1
CLOCK
RESET
CODE VCO
CODE VCO CH1
DOPPLER COMMAND LATCHES
CODE GEN AND CODE VCO LATCHES CH1
SYNC COMMAND
MUX CHANNEL
20 MS
RD
ADRE
μP
INTERRUPT
ADDRESS
CONTROL
MUX
COMPARATOR
CARRIER LOCK MONITOR
LPF A
LPF B
LPF C
LPF D
RESET
FREQUENCY DISCRIMINATOR
AM DET
TAU-DITHER DEMODULATOR
CODE POSITION
MUX CHANNEL
DITHER CLOCK CH2
CODE GEN A
CODE VCO A
CODE GEN B
CODE VCO B
CODE GEN C
CODE VCO C
CODE GEN D
CODE VCO D
CODE SEL A CH2
CODE VCO A CH2
CODE SEL B CH2
CODE VCO B CH2
CODE SEL C CH2
CODE VCO C CH2
CODE SEL D CH2
CODE VCO D CH2
CODE GEN AND CODE VCO LATCHES CH2
MASTER RESET
20 MS TIMING
CHIP ENABLE ADRESS DECODER
CE1
CE2
CE3
CE4
CE5
CE6
CE7
CE8
DITHER CLOCK GATE
DOPPLER COMMAND LATCHES
CODE GEN AND CODE VCO LATCHES CH2
MASTER RESET
SFR
2-7-80

BASELINE DESIGN COMPLETION

- COMPLETE TRADE-OFF STUDIES
- COMPLETE ELECTRICAL DESIGN AND GENERATE LIST-OF-MATERIALS
- CHOOSE CANDIDATE MECHANICAL DESIGN
- WORK WITH COLLINS DESIGN-TO-COST SECTION TO COME UP WITH LOW QUANTITY PRODUCTION COSTS
- WORK WITH GM TO DEVELOP HIGH VOLUME COST ANALYSIS
- COMPLETE RISK ASSESSMENT
- CONDUCT FINAL REVIEW
- DEVELOP FINAL DESIGN DEFINITION

ALTERNATE FUNCTIONAL DESIGN CHOICES

- DIGITAL CORRELATOR
- SINGLE CHANNEL SEQUENTIAL
- NONVOLATILE ELECTRONICALLY ERASABLE PROM
- LOW-POWER PROCESSOR
- SAW RESONATOR OSCILLATOR
- DIRECT CONVERSION RECEIVER
- MULTIPLEXED CODE GENERATOR
- POWER SUPPLY

TECHNICAL SUMMARY

- MAJOR EFFORT IS MINIMUM-COST DESIGN APPROACH
- BASELINE DESIGN NOW IN LOW-COST DESIGN CYCLE
- HARDWARE DESIGN NEARING COMPLETION
- MAJOR HARDWARE COST ELEMENTS IDENTIFIED
- ANTENNA SELECTION MADE
- LSI LOOKS FEASIBLE FOR MAJOR PORTIONS OF RECEIVER HARDWARE
- PRELIMINARY SIZE AND POWER ESTIMATES COMPLETED
- FINAL REPORT OUTLINE DEVELOPED
- ENVIRONMENTAL REQUIREMENTS NEED FINALIZATION
- MECHANICAL DESIGN CANDIDATES DEVELOPED AND AWAITING EVALUATION FOR HIGH VOLUME PRODUCTION
- GM HELP NEED FOR HIGH VOLUME FINAL COST DETERMINATION

FINAL REPORT OUTLINE

1. INTRODUCTION
2. EXECUTIVE SUMMARY
3. GPS SYSTEM OVERVIEW
4. SYSTEM DESIGN REQUIREMENTS
5. SYSTEM DESIGN ISSUES
6. GPS SIGNALS
7. LOW-COST DESIGN APPROACH
8. PRELIMINARY SYSTEM DEFINITION
   - ANTENNA
   - RECEIVER
   - PROCESSOR
   - MECHANICAL
9. ANTENNA DESIGN
10. RECEIVER DESIGN
11. PROCESSOR HARDWARE DESIGN
12. PROCESSOR SOFTWARE DESIGN
13. GPS SET POWER SYSTEM
14. MECHANICAL DESIGN
15. INTERFACE DEFINITIONS
16. COST ANALYSIS
17. TECHNOLOGY SUMMARY
18. TRADE-OFF STUDY SUMMARY
19. SYSTEM SPECIFICATION SUMMARY
20. SYSTEM PERFORMANCE SUMMARY
21. PHASE II & III PLANNING
22. APPENDIX

PERSONNEL TASKS AND MANNING LEVELS

NAME	TASKS	% OF REMAINING EFFORT
S.F. RUSSELL	- PROJECT MANAGER - SYSTEM CONCEPT - TECHNOLOGY - COST ANALYSIS - ANTENNA DESIGN - PHASE II & III PLANNING - FINAL REPORT	21
L.M. NIGRA	- HARDWARE DESIGN - LOW-COST ANALYSIS - TRADE STUDIES - TECHNOLOGY - RECEIVER DESIGN	27
R.W. WALSTROM	- PROCESSOR HARDWARE - PROCESSOR SOFTWARE - COST ANALYSIS - TRADE STUDIES	27
P.L. ROBERTS	- MECHANICAL DESIGN - ENVIRONMENT - LOOKING MODEL	20
R.H. POOL	- SYSTEM CONSULTING	5
		100%

SCHEDULE AND MANNING

- PROGRAM COMPLETION RATE

- PERSONNEL TASKS AND MANNING LEVELS

PROGRAM COMPLETION RATE